EEE 230 Online
Assign 6

1. There are 4 caches with the organization and block size as indicated below. All caches hold 128 words where each word is 4 bytes. Assuming a 32-bit address.

   a. A direct-mapped cache with block size of 16 words
   b. 2-way set-associative cache with block size of 8 words
   c. 4-way set-associative cache with block size of 4 words
   d. A fully associative cache with block size of 32 words.

Complete the table for each cache.

	Cache a	Cache b	Cache c	Cache d
total # bits need for word + byte displacement				
# bits needed for index				
# bits needed for tag				
# bits (total) per set (including valid and dirty bits)				

2. Here is a series of addresses in <u>hexadecimal</u>:

   20(w), 3C(r), 10(r), 16(w), 20(r), 04(w), 28(r), 6(r), 10(w), 17(w)

   Assume a LRU replacement algorithm. For the four caches in problem 1, draw each cache as it would appear at the end of the series of references. Include the valid bit, dirty bit, and tag. Show the contents of the memory block using the byte address range such as M[20-23] for the word with address 22.

3. The memory hierarchy contains a single cache with a miss rate of 2% that holds both instructions and data. The miss penalty to access main memory is 100 cycles. 15% of the instructions are jumps, 20% are stores, 20% are loads (30% have values used in the next instruction), 10% are branches (taken 20% of the time) and 35% are ALU instructions. Jumps and branches are determined in the ID stage.

   a. What is the base CPI?
   b. What is the effective CPI?