DAYTONA STATE COLLEGE
COLLEGE OF ENGINEERING TECHNOLOGY
CET 3116 DIGITAL TECHNOLOGY

LAB PROJECT - 2

OBJECTIVES:

Design and simulate a 4-bit Synchronous Up-Down Counter in Quartus II.

DESCRIPTION:

This project is an individual assignment. Students will work with Quartus II graphic design tool and simulator that was used in Project 1. The project covers design and simulation of sequential circuits, specifically, four-bit Up-Down counter.

GUIDELINES:

1) Lab projects (Project 1 + Project 2) will account of 100% of the labs and projects grade.
2) Each student will turn in a report with the results of their design and simulation of the circuits accompanied with supporting files. The report should contain:

    a) Title Page The title page should be a single page with only the following. information:
        i) Course number with section
        ii) Project title
        iii) Your name and IDs
        iv) The date the project is submitted.
        v) A brief description of the project
    b) Theory of operation: Explain how your circuit works, but do not give implementation details. This should be an expanded version of the introduction. That is to give a high level description of what your circuits do and how they do it. For example, you could explain any algorithms you implemented, any conditions or restrictions the user must observe to use the circuits, and the high level structure of your circuits at the block diagram level.
    c) Design details: This subsection is where you can go into the details of your design. It should contain any logical expressions you use, any Karnaugh maps or algebraic simplifications you performed, and any tables or state diagrams for sequential circuits. It should explain design techniques if they are not self-explanatory. It should refer to the detailed documentation (such as schematic diagrams) explicitly. This section should also contain a description of any unusual problems you had and how you solved them.
    d) Schematic Diagrams. Make sure all input and output connectors are labeled with the proper signal name. Add labels for any interior signals that appear in the written description of the circuit, especially those that appear in logical expressions.
    e) The waveform resulting from the time simulation. Do as many simulations you consider that show the functionality of the circuit. You should set the waveform in the same order of variables that you provide in the truth tables.
        i) Use only functional simulation.
    f) Analysis, including comments and conclusions.

3) For this second project, you will proceed with the design and simulation of a four-bit Up-Down counter; you will need to use Flip-Flops JK negative edge triggered 74112. The flip flops are available in .mf library. This flip flops come in Dual-Packages so all you need is two of them. Implementation with other class of devices, like 71LS161/163 will not be considered. You need to take into consideration the following:
   a) The simulations should use a clock of 25 MHz
   b) The snap shots should show a complete count (from 0000 to 1111 and another for a count from 1111 to 0000), and should show uses of Asynchronous Clear and Preset.
4) The project will be evaluated considering the following aspects:
   a) Result correctness.
   b) Report completeness.
   c) Clarity of ideas.
   d) Bonus points implementing with ALTERA boards DE2-115
5) Deadlines:
   a) A Drop-box will be available for uploading your report and Quartus II files. Only documents submitted as Microsoft Word (.doc or .docx) or .PDF formats will be considered for the report. Also you need to submit the respective design file (.BDF) and Waveform files (.VWF).
   b) Complete project due midnight July 25th 11:59 p.m. (Eastern Time).