CS M51A / EE M16

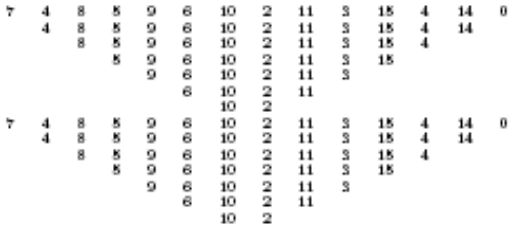
Winter 2016

Homework #5

Problem 1: Implement the following program repeatedly using a single 8-bit adder/subtracter (AS) module, 8-bit registers, as few as possible as small as possible counters and combinational modules of your choice.
The AS module executes addition, when control signal c1 is 0 and subtraction when control signal c1 is 1. Every five cycles the 7-bit input variables b, c, and e are updated with new values. All values (given and calculated) are positive. Values a, f, g, h, and d should be available one each clock cycle, in their respective order.

statement 1. a = b + c;
statement 2. f = b + e;
statement 3. g = a − c;
statement 4. h = b + e;
statement 5. d = b − c;

Problem 2: Using modulo 16 counters and multiplexers implement a system that produces the following sequence:



Problem 3: Design a system which outputs 1 if 4 of the last 5 characters are 1011 with at most 2 mismatched bits. The definition of mismatched bit is a bit in the sequence which doesn't correspond the its specified value. For example, for pattern 1111, the following sequences have 1 mismatched bit 0111, 1011, 1101, 1110. Use shift registers and minimal number of as small as possible multiplexers.

Problem 4: Using one 2-bit comparator module, design a system that sorts twelve 4-bit numbers. What is the minimal number of required clock cycles for your design to complete this task.

Problem 5: Four four-bit numbers (a, b, c, and d) and input signal x are given. Design a system which produces the sum of the two largest numbers if x = 0, and produces the sum

of the two smallest numbers if x = 1. Use at most one one-bit full-adder and only multiplexers for the required combinational logic.

Problem 6: A system receives a stream of data. Symbols a, b, c, and d form the stream. Design the system which finds the most popular (one most often generated) symbol called winner in each block of 32 input symbols. The system reports the number of winners and their value. Use only 2 data inputs multiplexers and shift registers.

Problem 7: Design a system that computes the following expression:

$$F = a*x^4 + b*x^3 + c*x^2 + d*x + e$$

The constant values a, b, c, d, and e are stored in five shift registers. Variable x arrives every 8 clock cycles. Use the minimal number of shift registers, multipliers, and adders to design the system.