CS3340 - Assignment 5
Pipelining and Memory Management (6% + 3% bonus)

Due 11:59pm, Sunday, 22 April 2017

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1. **Pipelining** (3% + 2% bonus)

   1.1. Forwarding (1.5%)

   Identify ALL of the data dependencies in the following code. Which dependencies are data hazards that can be resolved by forwarding? For each irresolvable data hazard, how many pipeline stalls will occur and in which instruction?

```
add $12, $15, $14
lw  $15, 100($12)
sub $13, $15, $12
add $12, $15, $13
```

   1.2. Stall Analysis (1.5%)

   In the class, we have shown how to *maximize* performance on our pipelined datapath with forwarding and stalls on a use following a load. Rewrite the following code to *minimize* performance on this datapath – that is, reorder the instructions so that this sequence takes the *most* clock cycles to execute while still obtaining the same result:

```
lw  $3,  0($5)
lw  $4,  4($5)
add $7,  $7,  $3
add $8,  $8,  $4
add $10, $7,  $8
sw  $6,  0($5)
beq $10, $11, loop
```

   1.3. Branch Hazards (2% bonus)

   One extension of the MIPS instruction set architecture has two new instructions called `movn` (move if not zero) and `movz` (move if zero). For example, the instruction

```
movn $8, $11, $4
```

   copies the contents of register 11 into register 8, provided that the value in register 4 is nonzero (otherwise it does nothing). The `movz` instruction is similar but copying takes place only if the register's value is zero. Show how to use the new instructions to put whichever is larger, register 8's value or register 9's value, into register 10. If the values

are equal, copy either into register 10. You may use register 1 as an extra register for temporary use. Do not use any conditional branches.

2. **Cache Performance** (3% + 1% bonus)

   2.1. (1.5%)

   Here is a series of address references given as word addresses: 2,3,11,16,21,13,64,48,19,11,3,22,4,27,6, and 11, show the hits and misses and final cache contents for a two-way set-associative cache with one-word blocks and a *total size* of 16 words. Assume LRU replacement.

   2.2. (1.5%)

   Using the series of references given in 4.1, show the hits and misses and final cache contents for a fully associative cache with one-word blocks and a *total size* of 16 words. Assume LRU replacement.

   2.3. (1% bonus)

   Using the series of references given in 4.1, show the hits and misses and final cache contents for a fully associative cache with four-word blocks and a *total size* of 16 words. Assume LRU replacement.

- **SUBMISSION:**

  You should store your written answers to these questions in one SINGLE file called "X.txt", or “X.doc”, where "X" is your last name (use only the first eight characters if it is more than eight). Clearly mark your name, student number, and detailed answers to the five question parts. Submit your file through eLearning to the assignment 5 site.

  There will be no extension of the deadline and late submissions will be penalized (1% deducted for each day delay and no submissions accepted after 3-day delay). Late submissions should be sent to the TA via email.

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